



GEN series

16/32 Channel Accel Card 250 kS/s

Features and Benefits

- 16 or 32 channels
- 250 kS/s sample rate/channel
- 1800 MB memory per card
- Programmable input amplifier
- 20 mV to 40 V input range
- Programmable filters
- Differential inputs
- 24 bit resolution
- IEPE and charge support
- TEDS status read out
- Digital I/O and one counter/timer

16/32 Channel Accel Card 250 kS/s

These cards have been developed for use in the five following application areas:

As a **differential amplifier**, they can be used in electrically **noisy environments**.

The CMRR of our true differential amplifiers ensures high signal fidelity.

Although not isolated they can be used as **entry level electrical input amplifiers** to measure electrical signals (voltage drops over shunts) with high impedance to ground.

For demanding applications we recommend use of one of our fully isolated amplifiers.

In **Accelerometer mode**, they offer excellent price/performance inputs for an array of IEPE based sensors (accelerometers, microphones, etc.).

Application features such as; High dynamic range using 24 bit A/D converter, excellent band-pass flatness up to a 100 kHz bandwidth, ensure phase alignment and amplitude accurate measurements.

In **Charge mode** they can be used directly with charge type sensors e.g. piezoelectric accelerometers or pressure transducers.

In **Single ended mode** the cards can serve as a cost effective coupler input for preconditioned signals to be recorded with the GEN DAQ series of products. In all modes the 16 and 32 channel Accel cards offer unmatched performance.

Capabilities Overview			
Component		Value	
Model		GN3210	GN1610
Sample rate max		250 kS/s	250 kS/s
Memory per card		1800 MB	1800 MB
ADC resolution ⁽¹⁾		16/24 bits	16/24 bits
Analog channels		32	16
Digital event channels ⁽²⁾		16	16
Timer/Counter support ⁽²⁾⁽³⁾		yes	yes
Input type			
	Analog	yes	yes
	IEPE	yes	yes
	Charge	yes	yes
	TEDS support ⁽⁴⁾	yes	yes

- (1) Software selectable
- (2) When supported by mainframe
- (3) When in 24-bit mode
- (4) When IEPE selected

Note *The listed specifications are valid for cards that are calibrated, and used in the same mainframe and slot as they were at the time of the calibration. When the card is removed from its original location and placed in another slot and/or mainframe the following specifications are invalidated: Offset error, gain error and MSE. Typically they can double.*

General Specifications					
Analog and Global					
Component		Unit Description		Value	
Channels				GN3210	GN1610
				32	16
Input connectors		D-Sub (DD-50) connector		2	1
Input type		Differential (software switchable to single-ended positive or negative), symmetrical		DC, AC, GND	
Input ranges		Given voltage spans apply where offset = 0		± 10 mV, ± 20 mV, ± 50 mV, ± 100 mV, ± 200 mV, ± 500 mV, ± 1 V, ± 2V, ± 5 V, ± 10 V, ± 20 V	
Offset		Zero position (except for the 40 V range)		± 50 % Full scale	
Offset error drift				± (10 ppm + 2 µV)/°C	
Input impedance				2 x 1 MΩ (± 0.5 %) // 2 x 75 pF (± 15 %)	
Max static error		Total		± 0.015 % ± 25 µV	
Gain error				± 0.015 % ± 25 µV	
Gain error drift				± 10 ppm/°C	
Noise		Total		± 0.01 % ± 25 µV	
CMRR		In range <4 V		< -80 dB	
		In range ≥4 V		< -60 dB	
CMV		In range <4 V		± 3 V _{peak}	
		In range ≥4 V		± 50 V _{peak}	
Input protection				± 50 V _{peak}	
Sample rate		High rates		10 S/s to 250 kS/s	
		Low rates (Low rate = High rate / n, where n is an integer ≥ 2)		1 S/s to 125 kS/s	
Binary sample rate		Supported		Yes	

General Specifications

Analog and Global

Component	Unit Description	Value
External time base	Supported	Yes
Filter selection		
Bandwidth	250 kS/s and 125 kS/s (Sigma Delta wideband selected)	100 to 105 kHz @ -3 dB
	Bandwidth @ All other sample rates	80 to 85 kHz @ -3 dB
	Flatness up to 100 kHz	In range < 4 V +0 dB/-0.3 dB In range ≥ 4 V +0.2 dB/-0.4 dB
Digital Decimation Filters		
Time Domain	12 ⁽¹⁾ -pole Bessel style IIR, sample rate divided by 10, 20, 40 and 100	
	Minimum filter frequency	40 Hz @ -3dB
Frequency Domain	12-pole Butterworth style IIR, sample rate divided by 4, 10, 20 and 40	
	Minimum filter frequency	100 Hz @ -3dB
Measurement category	IEC 61010	CAT 1

(1) Bessel style IIR filter frequencies, 25 kHz and 20 kHz are 8-pole.

Sigma Delta Wideband Characteristics

Component

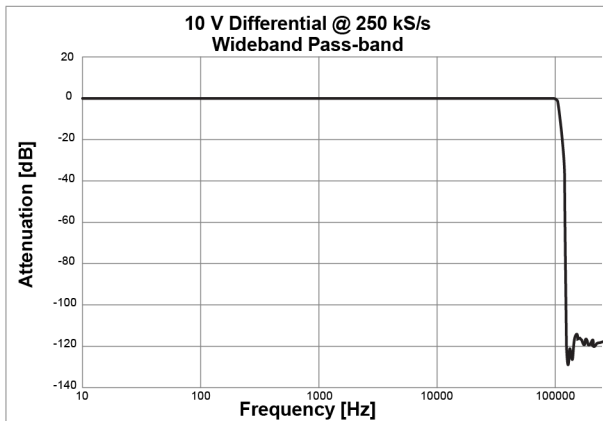


Figure 1.1: 10 V Differential @250 kS/s

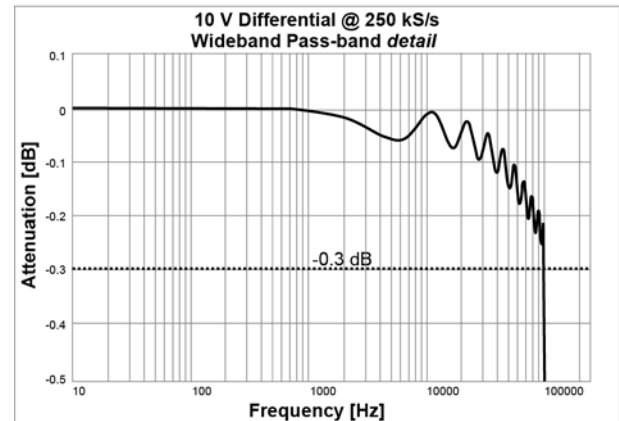


Figure 1.2: 10 V Differential @250 kS/s - Detail

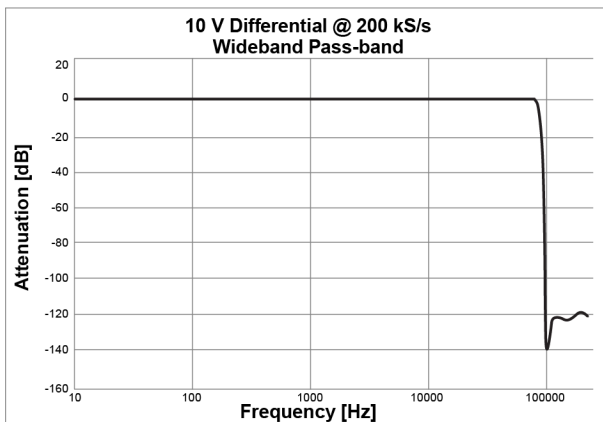


Figure 1.3: 10 V Differential @200 kS/s

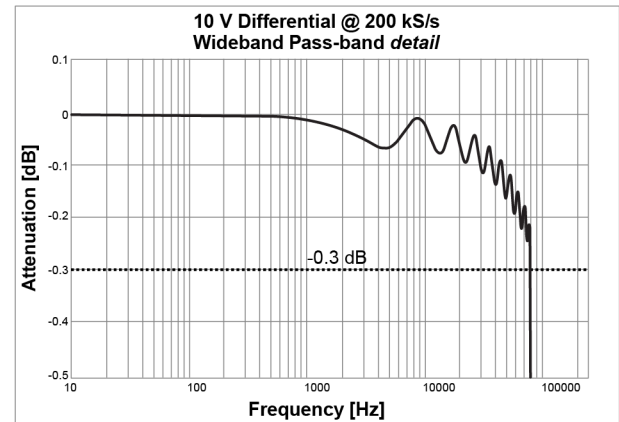


Figure 1.4: 10 V Differential @200 kS/s - Detail

IEPE Amplifier		
Component	Unit Description	Value
Input ranges		± 10 mV, ± 20 mV, ± 50 mV, ± 100 mV, ± 200 mV, ± 500 mV, ± 1 V, ± 2 V, ± 5 V, ± 10 V, ± 20 V
Over voltage protection		-1 V to 22 V
IEPE gain error	All ranges	± 0.1 % ± 300 μ V
IEPE gain error drift		± 10 ppm/ $^{\circ}$ C
Sensor compliance voltage		22 V
Sensor excitation current	Software selectable	2 mA, 4 mA, 6 mA and 8 mA
	Excitation accuracy	± 5 %
	Coupling time constant	1.5 s
	Lower bandwidth	-3 dB @ 0.11 Hz
	Sensor ID readout	TEDS
	Maximum cable length	100 m (RG-58)

Charge Amplifier		
Component	Unit Description	Value
Input ranges		± 10 pC, ± 20 pC, ± 50 pC, ± 100 pC, ± 200 pC, ± 0.5 nC, ± 1 nC, ± 2 nC
Over voltage protection		± 30 V _{peak}
Charge gain error		± 2 %
Charge gain error drift		± 30 ppm/ $^{\circ}$ C
Lower bandwidth limit		-3 dB @ 1 Hz
Upper bandwidth limit	1 nF source capacity	-3 dB @ 10 kHz

Digital Functionality		
<i>Only available when the mainframe provides a complementary connector</i>		
Component	Unit Description	Value
Event inputs		
	Number of	16
	Levels	User can invert value in software High (1)/Low (0)
Event/Status outputs		
	Number of	2
	Status output	Acquisition status High when active
	Event output	Trigger or Alarm; user programmable
Event out		
	Duration	Pulse of 12.8 μ s
	Delay	200 μ s ± 1 μ s ± 1 sample
Timer/counter functionality		
	Uses three event input channels. You can use timer/counter functionality in parallel with the used event input channels	<ul style="list-style-type: none"> ● Counter ● Frequency counter ● Quadrature decoder
Counter		
	Functionality	Up/down counter with reset
	Inputs	<ul style="list-style-type: none"> ● Count ● Up/down ● Reset
	Range	Count up or down with a 32-bit counter
	Frequency	Maximum input frequency
		0 - 4 294 967 295 (4 Gb)
		5 MHz

Digital Functionality

Only available when the mainframe provides a complementary connector

Component		Unit Description	Value
	Reset	One of four modes: <ul style="list-style-type: none"> • Software controlled (manual) • On Start of Acquisition • On external trigger once • Always on external trigger 	
Frequency counter			
	Functionality	Frequency and RPM measurement with external direction input and reset	
	Inputs	<ul style="list-style-type: none"> • Measure • Direction • Reset 	
	Frequency	Maximum input frequency	5 MHz
	Accuracy	Measurement accuracy	0.1 %
	Gate time	Measurement gate time, user selectable	5 ms to 50 s
	Reset	One of four modes: <ul style="list-style-type: none"> • Software controlled (manual) • On Start of Acquisition • On external trigger once • Always on external trigger 	
Quadrature decoder			
	Functionality	Quadrature decoding with reset	
	Inputs	<ul style="list-style-type: none"> • Signal A • Signal B • Reset 	
	Frequency	Maximum input frequency	5 MHz
	Accuracy	The number of edges in the input signals used per cycle to determine position.	1: Single precision 2: Dual precision 4: Quadruple precision
	Count	Maximum count equals counter width divided by precision 'N'	32 bit/N
	Reset	One of four modes: <ul style="list-style-type: none"> • Software controlled (manual) • On Start of Acquisition • On external trigger once • Always on external trigger 	
Status output			
	Functionality	Outputs status. One event for "Acquisition active" and one for "Trigger" or "Alarm" under user control	
	Outputs	<ul style="list-style-type: none"> • Acquisition active • Trigger/alarm 	
	Acquisition active	Active high when recording. Low in idle and pause mode	Level
	Pulse width	Trigger output pulse	12.8 µs
	Delay	Delay from actual event to output	200 µs ± 1 µs ± 1 sample

Triggering

Component		Unit Description	Value
Triggered acquisition		Pretriggered acquisitions, with user selectable pre- and post trigger	
Trigger detector		The trigger detector flags a user-defined situation on the input signal to start an acquisition sequence (trigger) or to arm the acquisition (qualifier). Digital functionality applies to event channels.	1 per channel
	Functionality	Analog trigger modes	2
		Digital trigger modes	1
		Digital qualifier modes	1
Levels	Analog: individual levels	2	
	Digital	1	

Triggering			
Component		Unit Description	Value
	Resolution	Analog: for each level; covers the selected Full Scale	16 bit (0.0015 %)
		Digital	1 bit
	Hysteresis	Defines the trigger levels insensitivity (analog only)	0.1 % to 100 % of FS
Pre-trigger length		Independent of storage medium used	0 to 100 % of recording length
Post trigger length		Sweepled acquisition	0 to full on-board RAM
		Continuous type acquisition	0 to full HD capacity
Trigger rate		Up to 400 triggers per second, with zero re-arm time	1 per 2.5 ms
Trigger total		Maximum number of triggers per recording	10,000
Cross-channel operation		Triggers of all channels	Logical OR
		Qualifiers of all event channels	Logical AND
Analog trigger modes			
	Basic	Single level	Positive or negative level crossing
	Dual level	Two individual levels, OR-ed	One positive and one negative level crossing
Digital (event) trigger modes			
	Basic	Single change of state	Rising or falling edge
Digital (event) qualifier modes			
	Basic	Arm the acquisition with a single change of state	Rising or falling edge

Acquisition and Storage Modes			
Component		Unit Description	Value
Modes			
	Sweeps	Triggered acquisition to an on-board Random Access Memory (RAM) without sample rate limitations.	
	Continuous	Direct triggered acquisition to a PC or mainframe hard disk without file size limitations. Triggered or untriggered.	
	Dual	Combination of sweeps and continuous mode: continuous type streaming acquisition to disk with simultaneously triggered sweeps in RAM.	
	Slow fast sweep	A triggered acquisition in RAM which includes an acquisition phase with a higher sample rate, located at a point of interest.	
	Sample width	When acquiring 16 bit data.	
When acquiring 24 bit data and/or using counter timer channels.			32 bit/sample
Acquisition			
	Sample memory		1800 MB

Front View

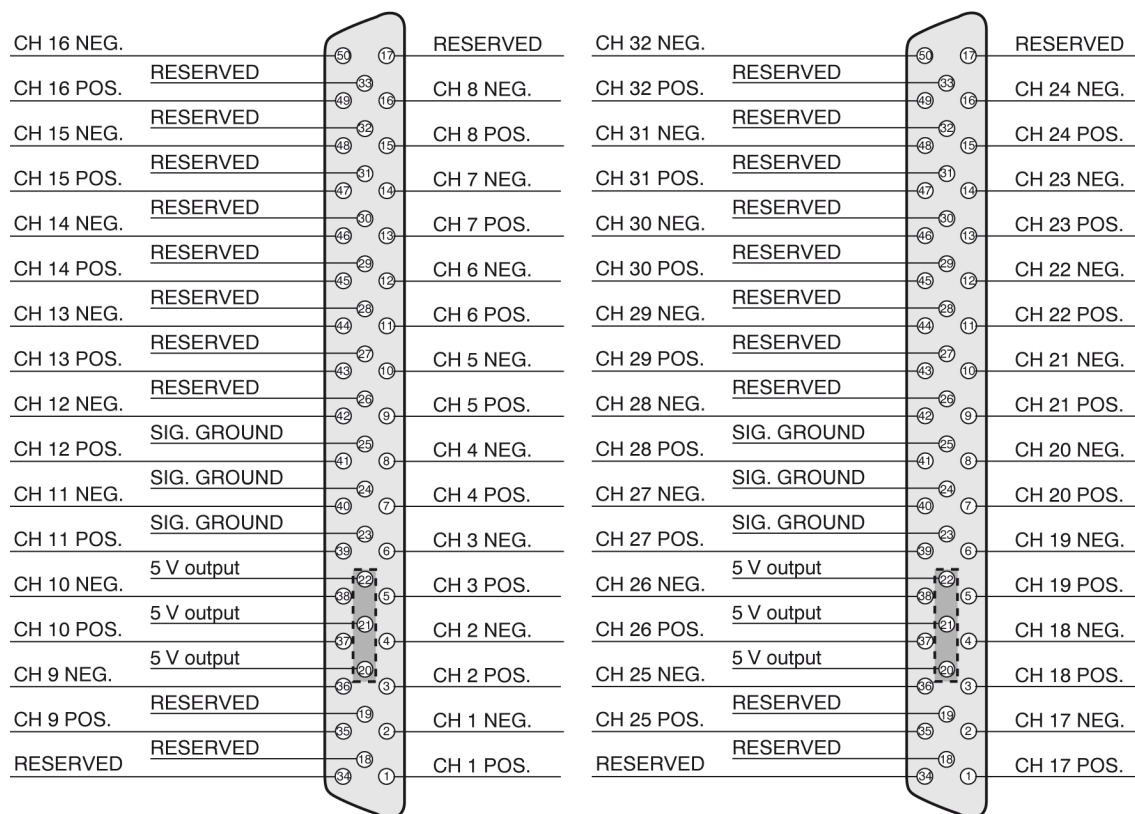



Figure 1.5: Pin diagram for top 16 Ch Connector (left), Bottom 16 Ch connector (right, 32 Ch Card only)

Note Both positive and negative pins must be connected to avoid erroneous measurement results with noise.

Note There are 3 output pins available on each connector giving 5 V at 0.3 A in total from an automatic resettable fuse.

Ordering Information			
Model		Unit Description	Order number
GN3210		32 Channel 250 kS/s per channel Differential digitizer, 1800 MB RAM per card, 16/24 bit, IEPE, TEDS and charge support	1-GN3210-2
GN1610		16 Channel 250 kS/s per channel Differential digitizer, 1800 MB RAM per card, 16/24 bit, IEPE, TEDS and charge support	1-GN1610-2

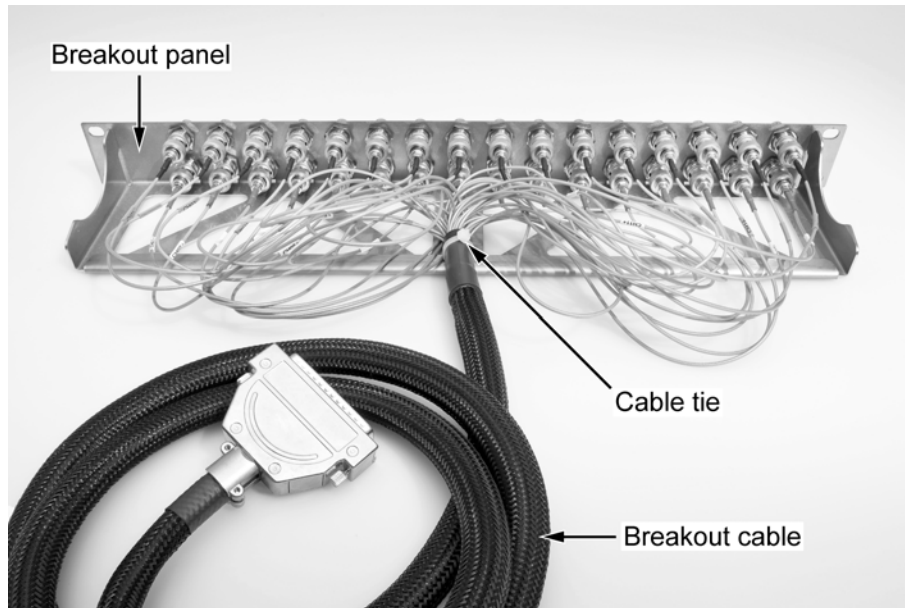




Figure 1.6: Breakout panel and cable

Accessories			
Model		Unit Description	Order number
KAB171		16 ch single ended break out cable, HDSUB to 16x BNC, 2 m; for use with GEN DAQ 16/32 ch input card	1-KAB171-1-2
KAB172		16 ch differential break out cable, HDSUB to 32x BNC, 2 m; for use with GEN DAQ 16/32 ch input card	1-KAB172-1-2
G055		16 ch single ended 19 inch or 1 U (44.45 mm) breakout panel; 16 BNC feed-through; to be used with 16 ch single ended break out cable	1-G055-2
G056		16 ch differential 19 inch or 1 U (44.45 mm) breakout panel; 16 x 2 BNC feed-through; to be used with 16 ch differential break out cable	1-G056-2
G058		32 ch single ended 19 inch or 1 U (44.45 mm) breakout panel; 32 BNC feed-through; to be used with two 16 ch single ended breakout cables	1-G058-2

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Hottinger Baldwin Messtechnik GmbH

Im Tiefen See 45 · 64293 Darmstadt · Germany
Tel. +49 6151 803-0 · Fax: +49 6151 803-9100
E-mail: info@hbm.com · www.hbm.com

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